# **Dual 3-Input 3-Output NOR** Gate

# Description

The MC10H211 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire ORing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10H211 particularly useful in clock distribution applications where minimum clock skew is desired.

#### **Features**

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 160 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K<sup>™</sup> Compatible
- Pb-Free Packages are Available\*

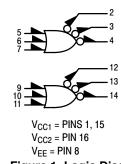
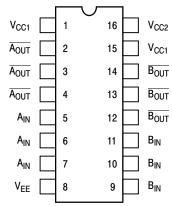


Figure 1. Logic Diagram



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

Figure 2. Dip Pin Assignment



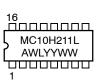
# ON Semiconductor®

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#### **MARKING DIAGRAMS\***



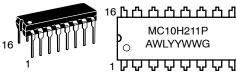
CDIP-16 **L SUFFIX** CASE 620A



MC10H211P

**AWLYYWWG** 

 $\overline{\Pi}$ 10H211 **ALYWG** 



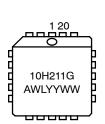
PDIP-16 P SUFFIX **CASE 648** 



SOEIAJ-16 **CASE 966** 



PLLC-20 **FN SUFFIX CASE 775** 



= Assembly Location

WL.I = Wafer Lot YY. Y = Year WW, W = Work Week = Pb-Free Package

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**Table 1. MAXIMUM RATINGS** 

Symbol	Characteristic	Rating	Unit
V <sub>EE</sub>	Power Supply (V <sub>CC</sub> = 0)	-8.0 to 0	Vdc
VI	Input Voltage (V <sub>CC</sub> = 0)	0 to V <sub>EE</sub>	Vdc
l <sub>out</sub>	Output Current - Continuous - Surge	50 100	mA
T <sub>A</sub>	Operating Temperature Range	0 to +75	°C
T <sub>stg</sub>	Storage Temperature Range - Plastic - Ceramic	−55 to +150 −55 to +165	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. ELECTRICAL CHARACTERISTICS (V<sub>EE</sub> = -5.2 V ±5%) (See Note 1)

		<b>0</b> °		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
Ι <sub>Ε</sub>	Power Supply Current	-	42	-	38	-	42	mA
I <sub>inH</sub>	Input Current High	-	720	-	450	-	450	μΑ
I <sub>inL</sub>	Input Current Low	0.5	-	0.5	-	0.3	-	μΑ
V <sub>OH</sub>	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V <sub>OL</sub>	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V <sub>IH</sub>	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
$V_{IL}$	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been
established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is
maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V. Note: If crosstalk is present, double bypass capacitor to 0.2 μF.

**Table 3. AC CHARACTERISTICS** 

		0° 25°		75°				
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
t <sub>pd</sub>	Propagation Delay	0.7	2.0	0.7	2.0	0.7	2.0	ns
t <sub>r</sub>	Rise Time	0.9	2.0	0.9	2.2	0.9	2.4	ns
t <sub>f</sub>	Fall Time	0.9	2.0	0.9	2.2	0.9	2.4	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC10H211FN	PLLC-20	46 Units / Rail
MC10H211FNG	PLLC-20 (Pb-Free)	46 Units / Rail
MC10H211FNR2	PLLC-20	500 / Tape & Reel
MC10H211FNR2G	PLLC-20 (Pb-Free)	500 / Tape & Reel
MC10H211L	CDIP-16	25 Unit / Rail
MC10H211M	SOEIAJ-16	50 Unit / Rail
MC10H211MG	SOEIAJ-16 (Pb-Free)	50 Unit / Rail
MC10H211MEL	SOEIAJ-16	2000 / Tape & Reel
MC10H211MELG	SOEIAJ-16 (Pb-Free)	2000 / Tape & Reel
MC10H211P	PDIP-16	25 Unit / Rail
MC10H211PG	PDIP-16 (Pb-Free)	25 Unit / Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# **Resource Reference of Application Notes**

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AN1672/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

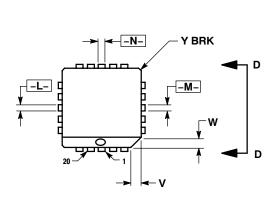
AND8020/D - Termination of ECL Logic Devices

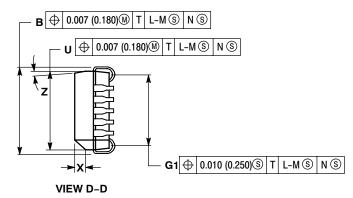
AND8066/D - Interfacing with ECLinPS

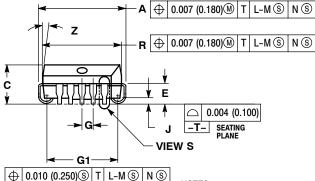
AND8090/D - AC Characteristics of ECL Devices

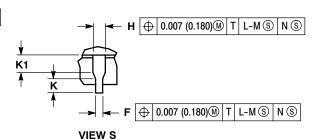
## PACKAGE DIMENSIONS

# **20 LEAD PLLC** CASE 775-02 **ISSUE E**









- NOTES:
  1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
- 1982.

  DIMENSIONS IN INCHES.

  DIMENSIONS IN INCHES.

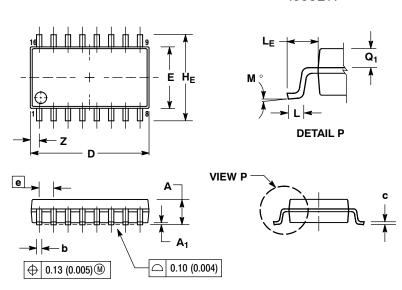
  DIFFERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

- PARTING LINE.
  4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM —T-, SEATING PLANE.
  5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
  6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- PLASTIC BODY.
  7. DIMENSION H DOES NOT INCLUDE DAMBAR DIMIENSION H DUES NOT INCLUDE DAMBAR
  PROTRUSION OR INTRUSION. THE DAMBAR
  PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION
  TO BE GREATER THAN 0.037 (0.940). THE DAMBAR
  INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO
  BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
С	0.165	0.180	4.20	4.57
Е	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020		0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
Х	0.042	0.056	1.07	1.42
Υ		0.020		0.50
Z	2°	10°	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

#### PACKAGE DIMENSIONS

# SOEIAJ-16 CASE 966-01 **ISSUE A**



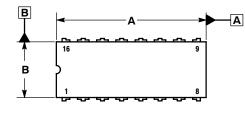
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI

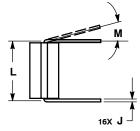
- NOTES:

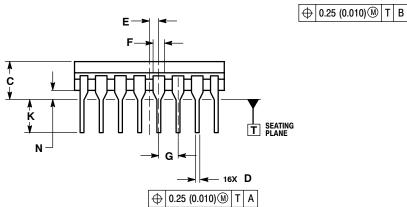
  1 DIMENSIONING AND TOLERANCING PER ANSI
  Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD
  FLASH OR PROTRUSIONS AND ARE MEASURED
  AT THE PARTING LINE. MOLD FLASH OR
  PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
  PER SIDE.
  4. TERMINAL NUMBERS ARE SHOWN FOR
  REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT
  INCLUDE DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
  TOTAL IN EXCESS OF THE LEAD WIDTH
  DIMENSION AT MAXIMUM MATERIAL CONDITION.
  DAMBAR CANNOT BE LOCATED ON THE LOWER
  RADIUS OR THE FOOT. MINIMUM SPACE
  BETWEEN PROTRUSIONS AND ADJACENT LEAD
  TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A <sub>1</sub>	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
С	0.10	0.20	0.007	0.011	
D	9.90	10.50	0.390	0.413	
E	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050 BSC		
HE	7.40	8.20	0.291	0.323	
L	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
M	0 °	10°	0 °	10°	
Q <sub>1</sub>	0.70	0.90	0.028	0.035	
Z		0.78		0.031	

# CDIP-16 **L SUFFIX** CERAMIC DIP PACKAGE CASE 620A-01 **ISSUE O**







#### NOTES:

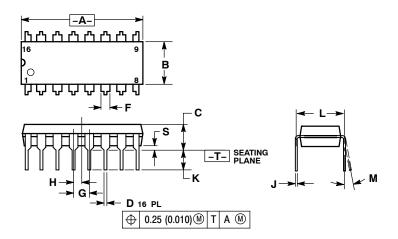
- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION LTO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
- BODY.
  THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620-10.

	INCHES		MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
C		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300 BSC		7.62	BSC	
M	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

## PACKAGE DIMENSIONS

PDIP-16 CASE 648-08 **ISSUE T** 



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
  DIMENSION L TO CENTER OF LEADS
  WHEN FORMED PARALLEL.
  DIMENSION B DOES NOT INCLUDE
- MOLD FLASH. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54	2.54 BSC	
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
٦	0.295	0.305	7.50	7.74	
М	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

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